EE 330
Lecture 12

Back-End Processing

Semiconductor Processes

Devices in Semiconductor Processes

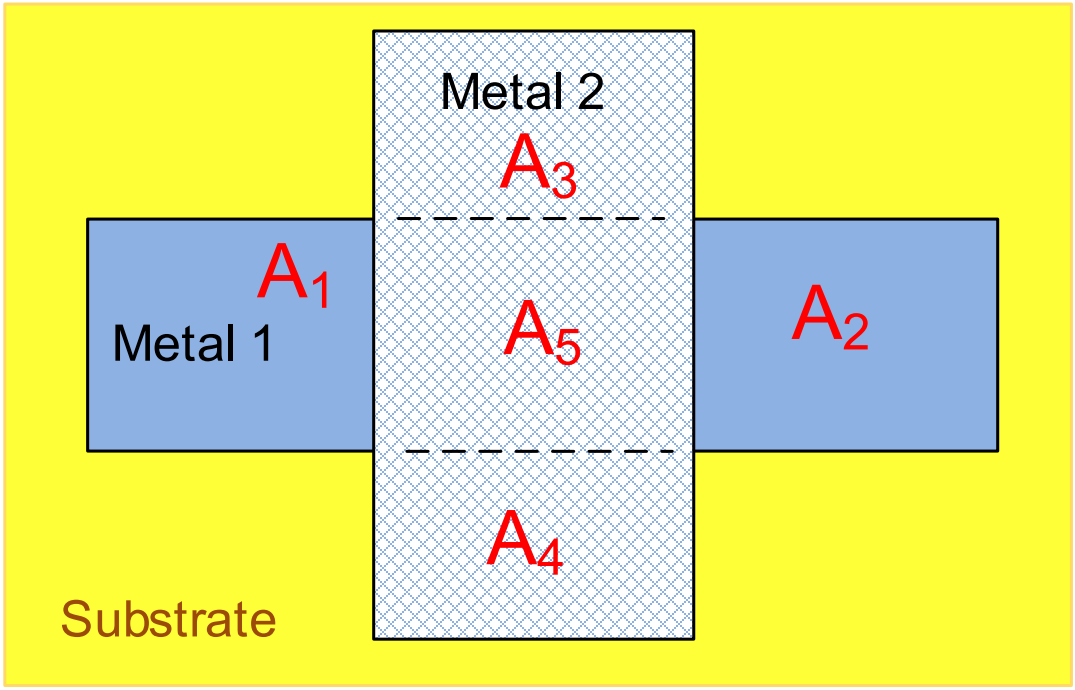
- Resistors
- Diodes
- Capacitors
- MOSFET
- BJT

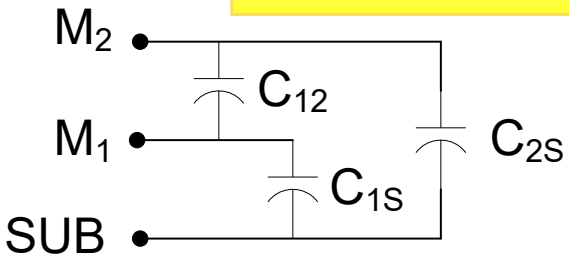
Fall 2025 Exam Schedule

Exam 1 Friday Sept 26

Review from Last Lecture

Capacitance in Interconnects





$$C_{12}=CD_{12}\,A_5$$

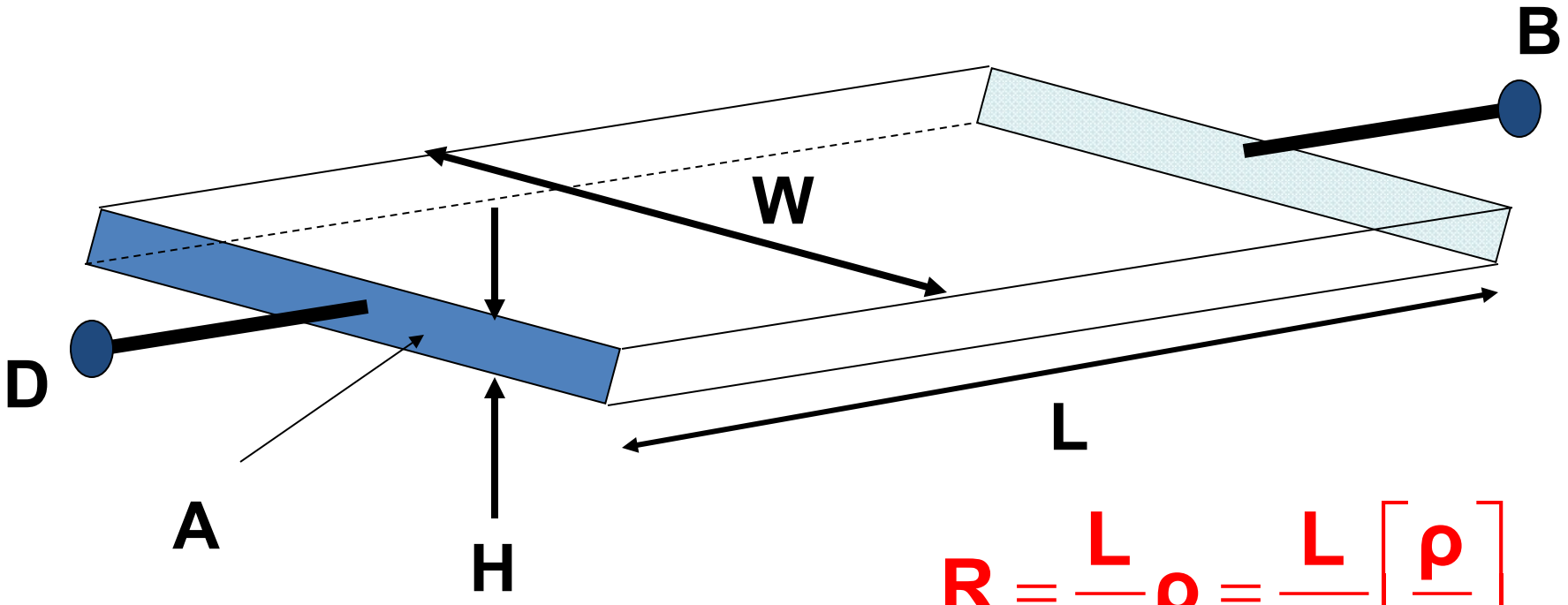
$$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Equivalent Circuit

Review from Last Lecture

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

Review from Last Lecture

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

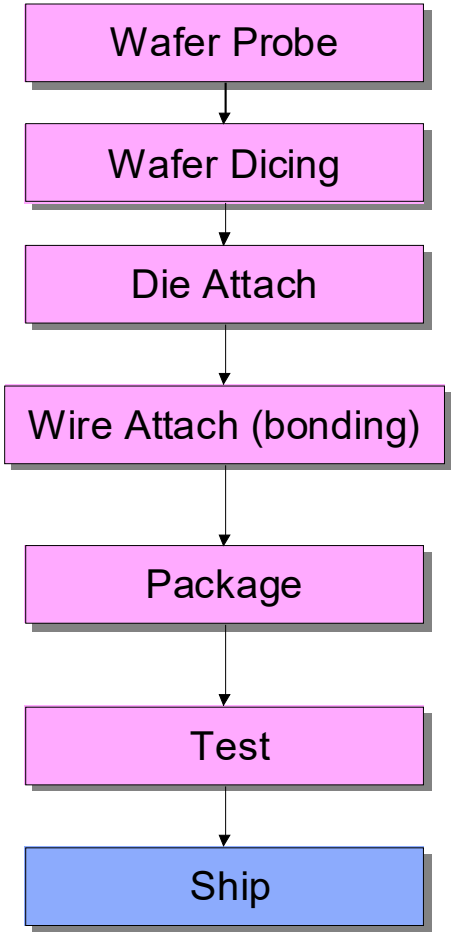
COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

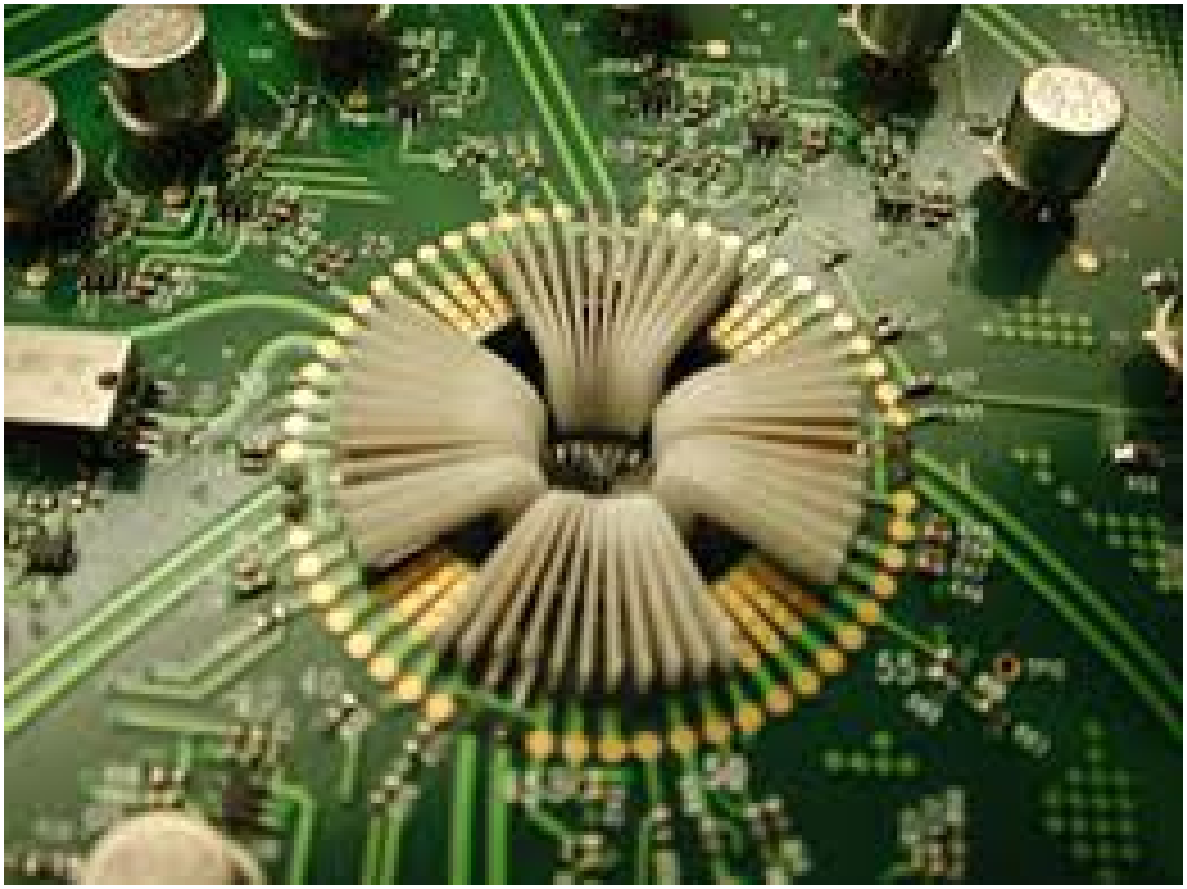
CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Review from Last Lecture

Back-End Process Flow



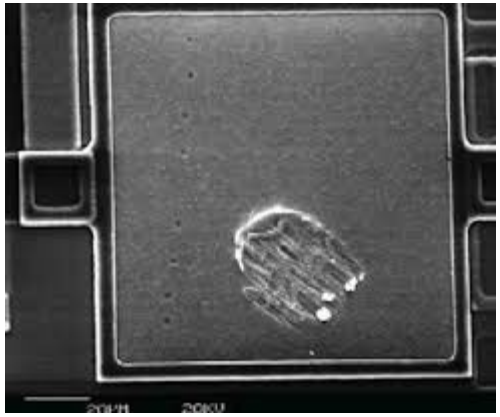
Probe Test



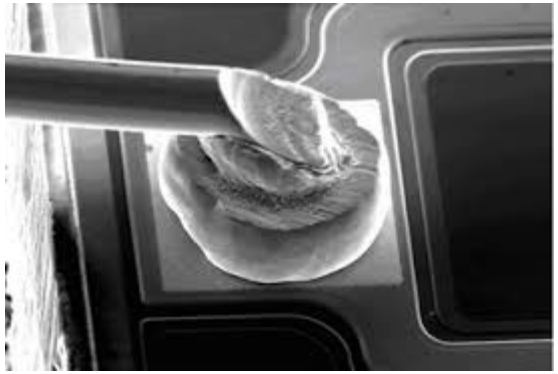
Probes on section of probe card

Photos from www postings and Google image search

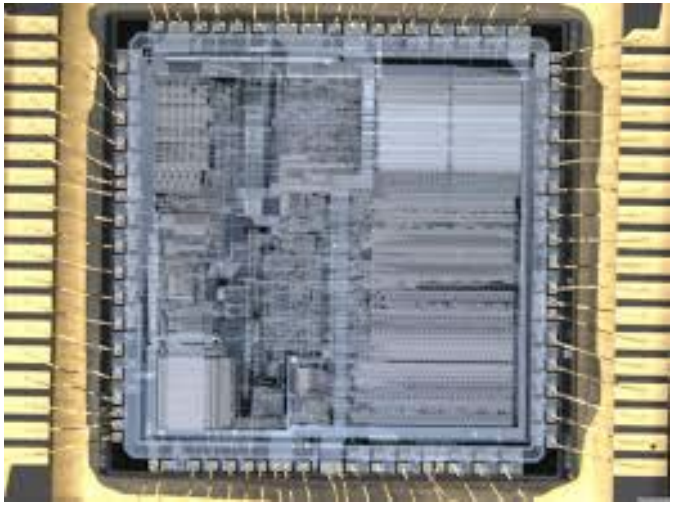
Probe Test



Pad showing probe marks



Pad showing bonding wire



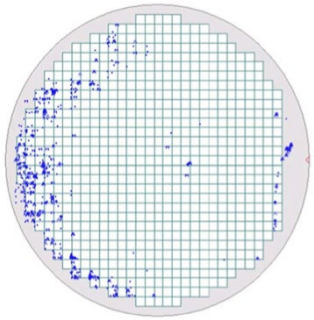
Die showing wire bonds to package cavity

Photos from www postings and Google image search

Probe Test

Production probe test facility

Goal to Identify
defective die on wafer



Photos from www postings and Google image search

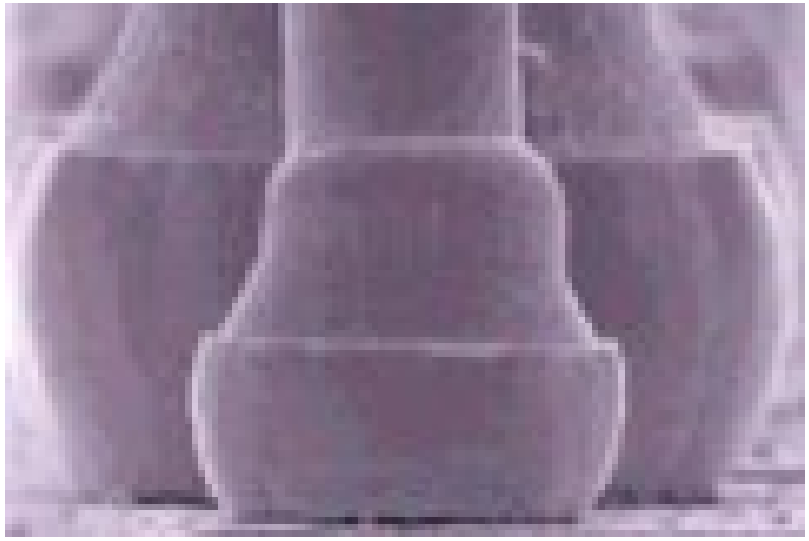
Review from Last Lecture

Die Attach

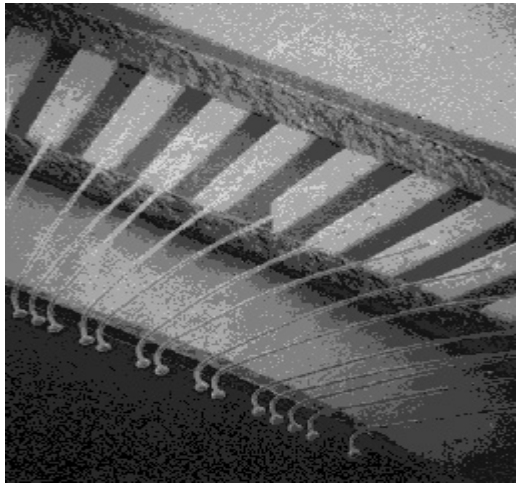
1. Eutectic
2. Pre-form
3. Conductive Epoxy

Review from Last Lecture

Wire Bonding

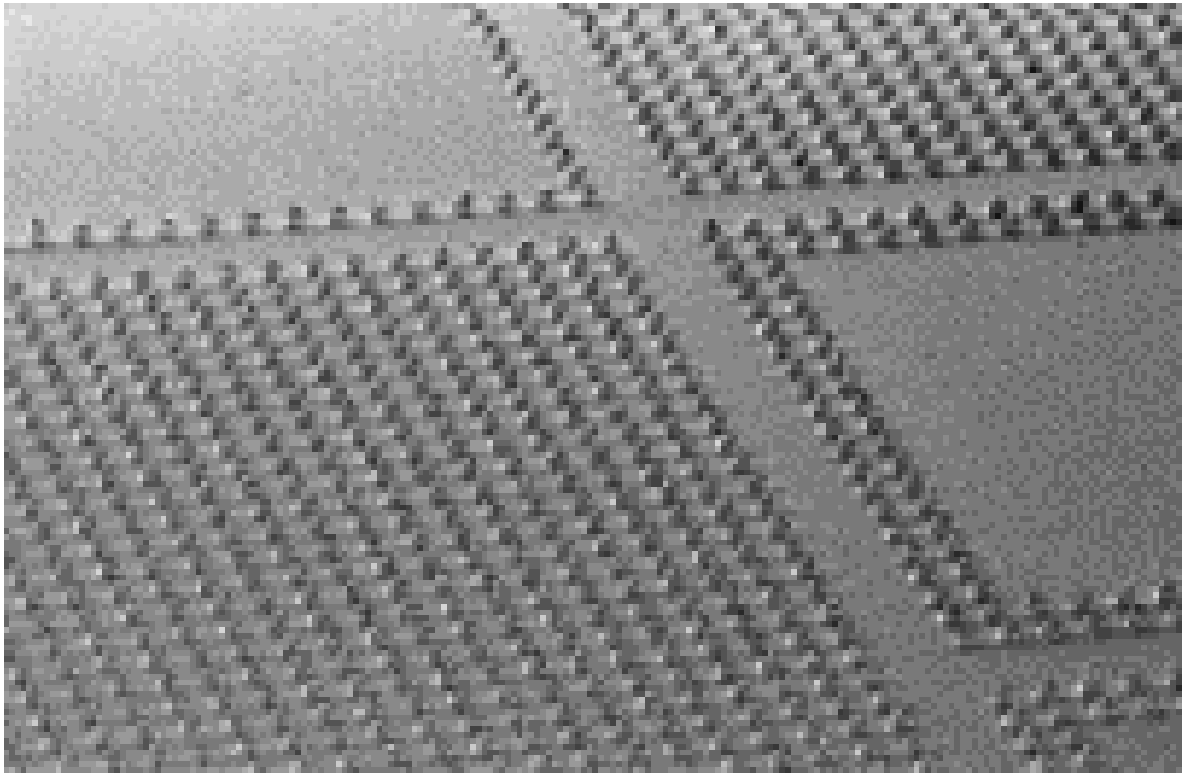


Ball Bond



Ball Bond Photograph

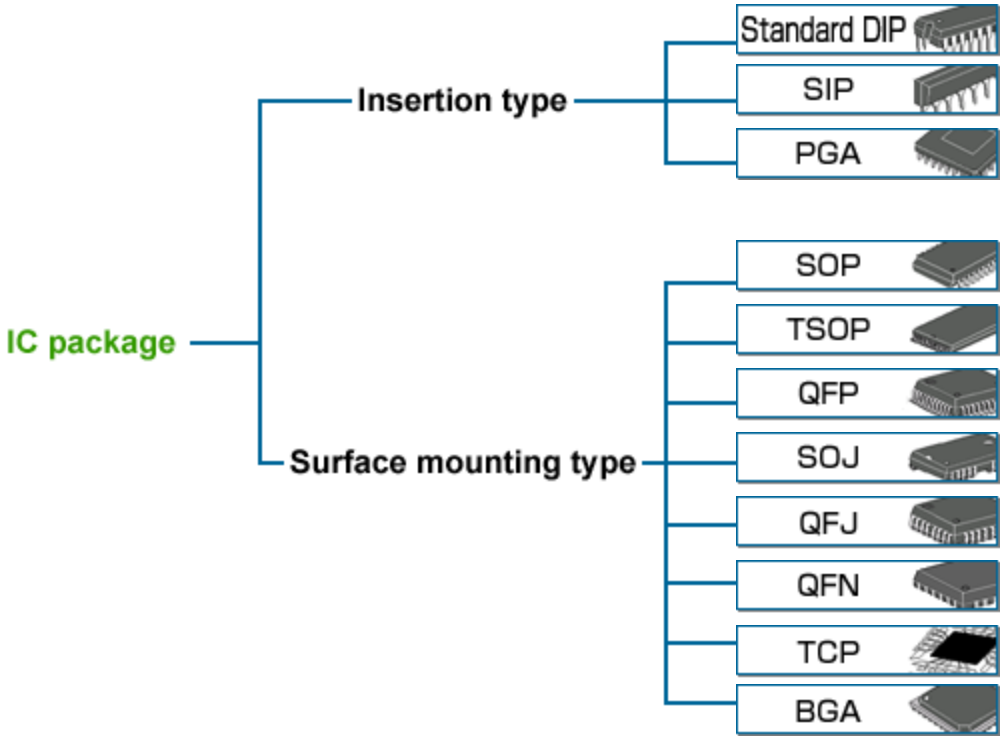
Bump Bonding



Packaging

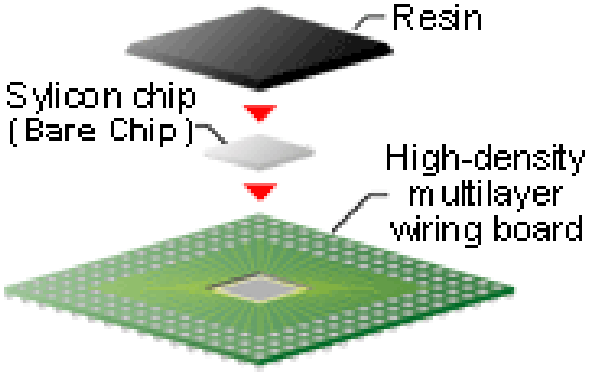
1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

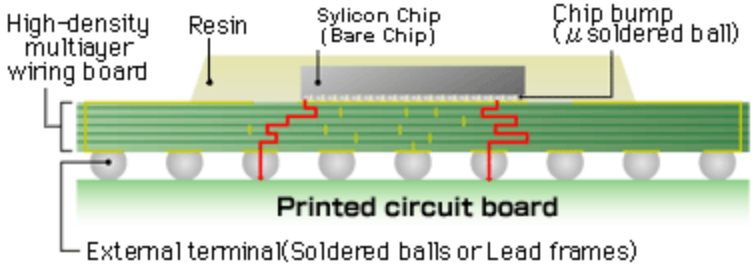
Packaging



www.necel.com

Packaging



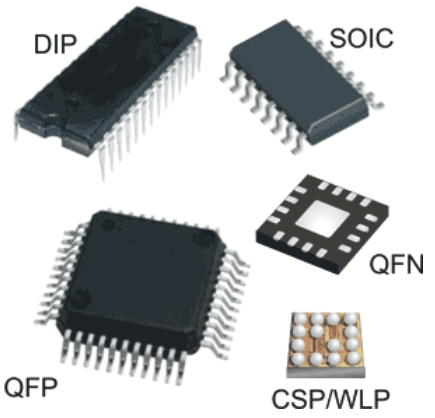


www.necel.com

Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

Name	Pin pitch	Size	Height
DIP or DIL	2.54		
SOIC-16	1.27	3.9 x 10	1.72
SSOP	0.635		
TSSOP54-II	0.8	12.7 x 22.22	~1
PLCC44	1.27		
PQ208[1]	0.50	28 x 28	3.4
TQFP64	0.40	7 x 7	1.0
TQFP144[2]	0.50	20 x 20	1.0
128PQFP	0.50	23.23 x 14.0	3.15



http://www.electroiq.com/index/display/packaging-article-display/234467/articles/advanced-packaging/volume-14/issue-8/features/the-back-end-process/materials-and-methods-for-ic-package-assemblies.htm

From Wikipedia, Sept 20, 2010

http://en.wikipedia.org/wiki/List_of_chip_carriers

Many standard packages available today:

http://www.interfacebus.com/Design_Pack_types.html

BCC: Bump Chip Carrier
BGA: Ball Grid Array; BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, CPGA Graphic
CQFP: Ceramic Quad Flat Pack, CQFP Graphic
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fpBGA: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) J-Lead Picture
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier LCC Graphic
LCC: Leaded Chip Carrier Un-formed LCC Graphic
LCCC: Leaded Ceramic Chip Carrier;
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, LGA uP [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leaded Chip Carrier LLCC Graphic
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier

PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack QFP Graphics
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SO Flat Pack: Small Outline Flat Pack IC
SOJ: Small-Outline Package [J-Lead]; J-Lead Picture
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack

Considerable activity today and for years to come on improving packaging technology

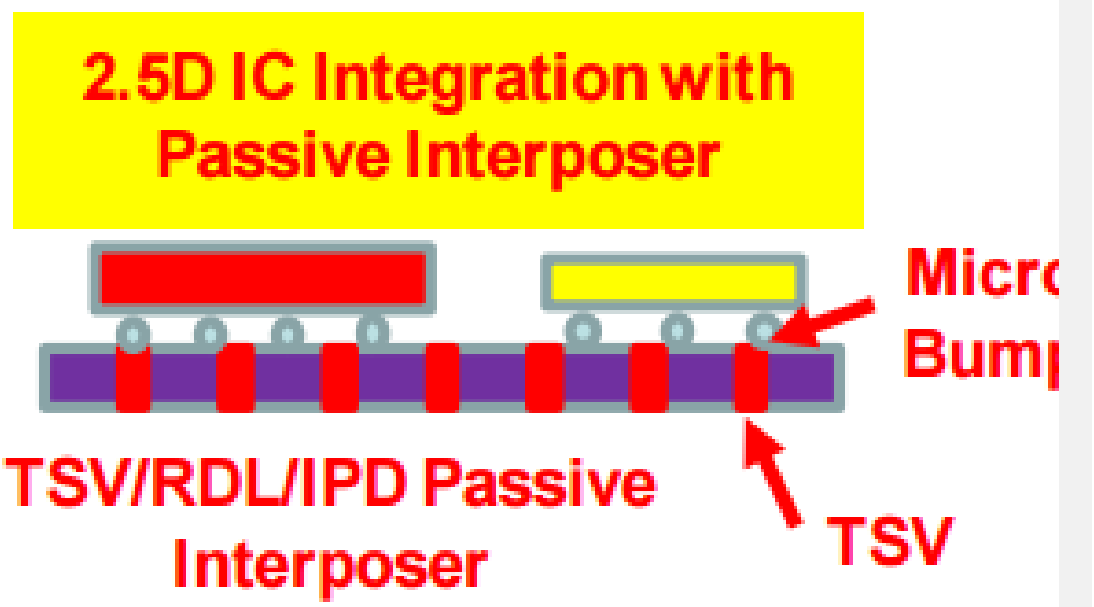
- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained

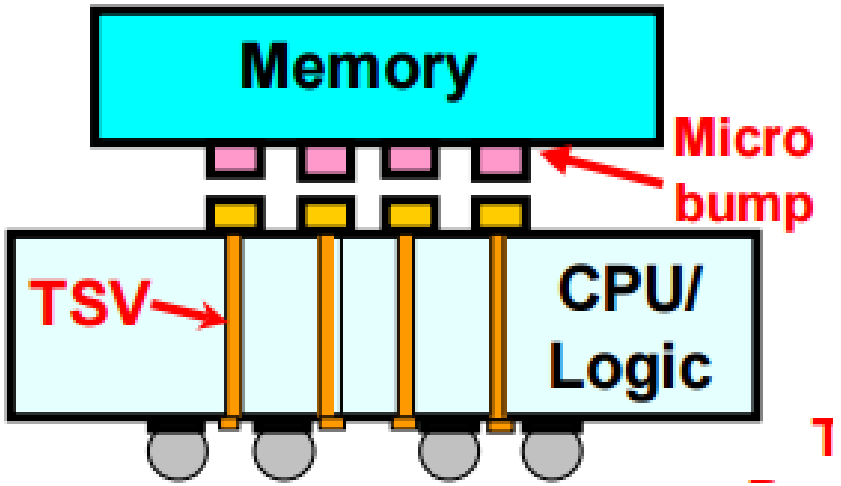
The following few slides come from a John Lau presentation

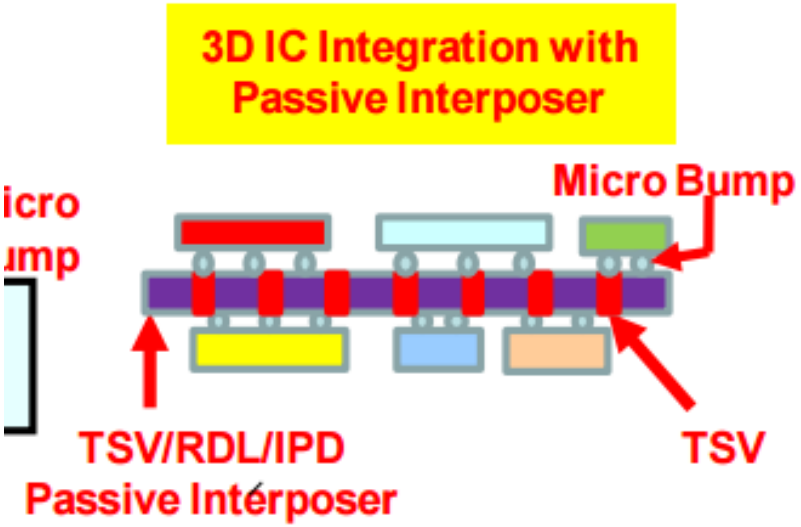
www.sematech.org/meetings/archives/symposia/10187/Session2/04_Lau.pdf

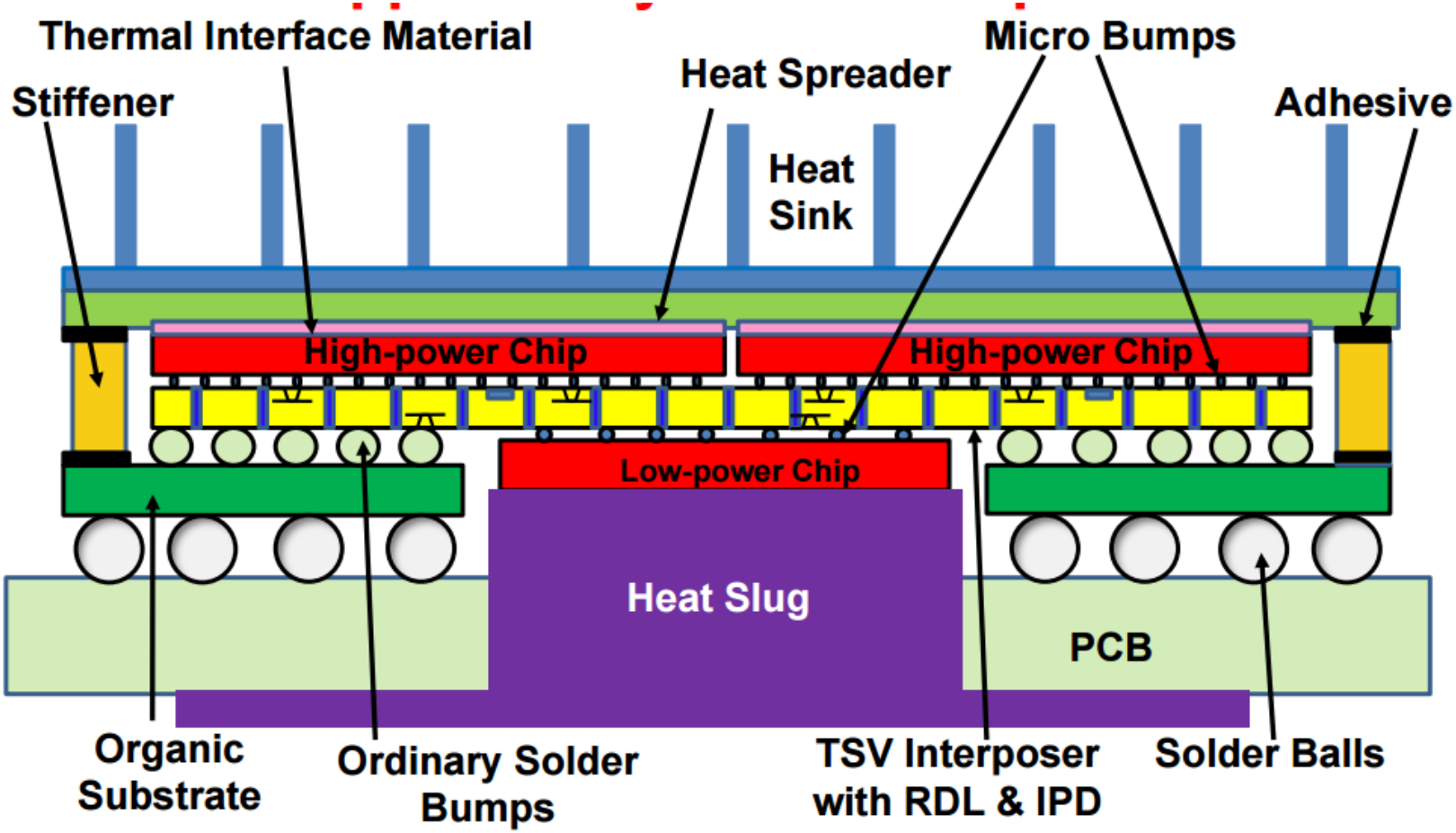
TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration

John H. Lau
Electronics & Optoelectronics Research Laboratories
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan 310, R.O.C.
886-3591-3390, johnlau@itri.org.tw

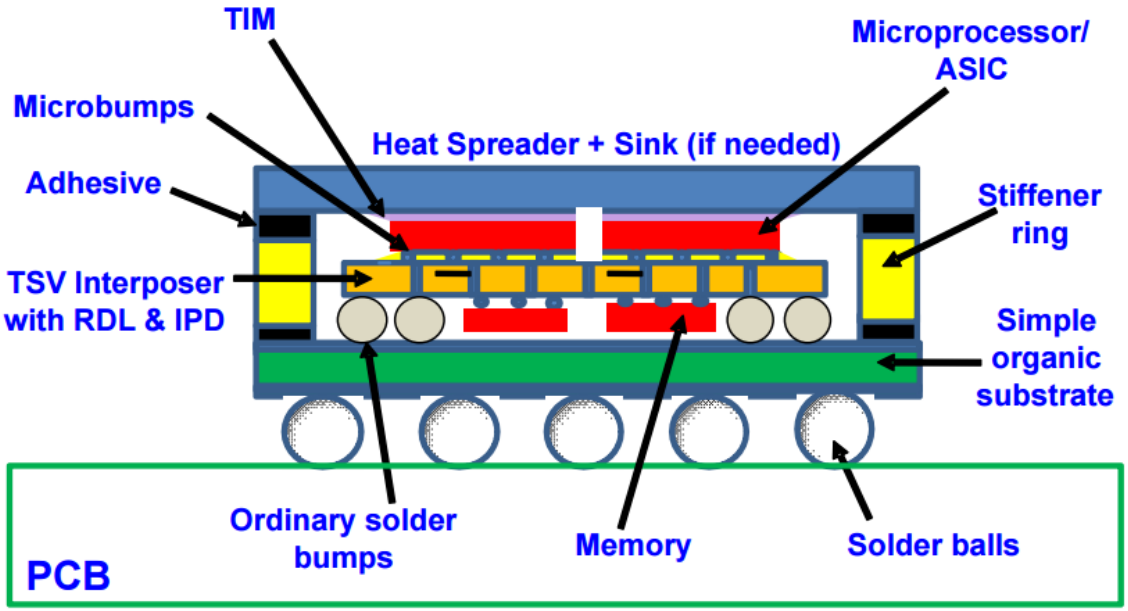

2.5D IC Integration with Passive Interposer
Micro Bump
TSV/RDL/IPD Passive Interposer
TSV


Memory
Micro
bump
TSV
CPU/
Logic


3D IC Integration with
Passive Interposer
Micro Bump
TSV/RDL/IPD
Passive Intérposer
TSV

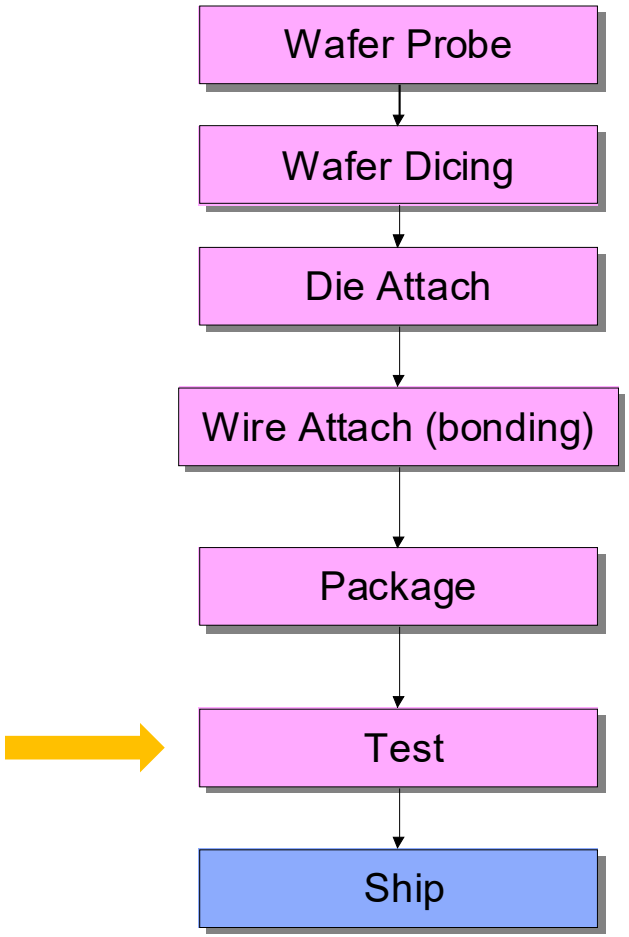

Thermal Interface Material
Stiffener
Heat Spreader
Micro Bumps
Adhesive
Heat
Sink
High-power Chip
High-power Chip
Low-power Chip
Heat Slug
PCB
Organic
Substrate
Ordinary Solder
Bumps
TSV Interposer
with RDL & IPD
Solder Balls

TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side



Special underfills are needed between the Cu -filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.

Back-End Process Flow



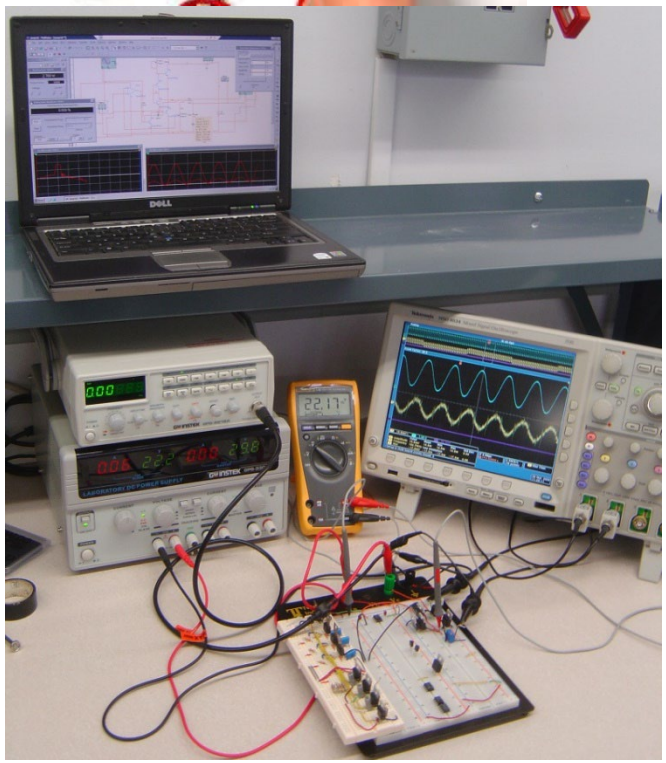
Testing of Integrated Circuits

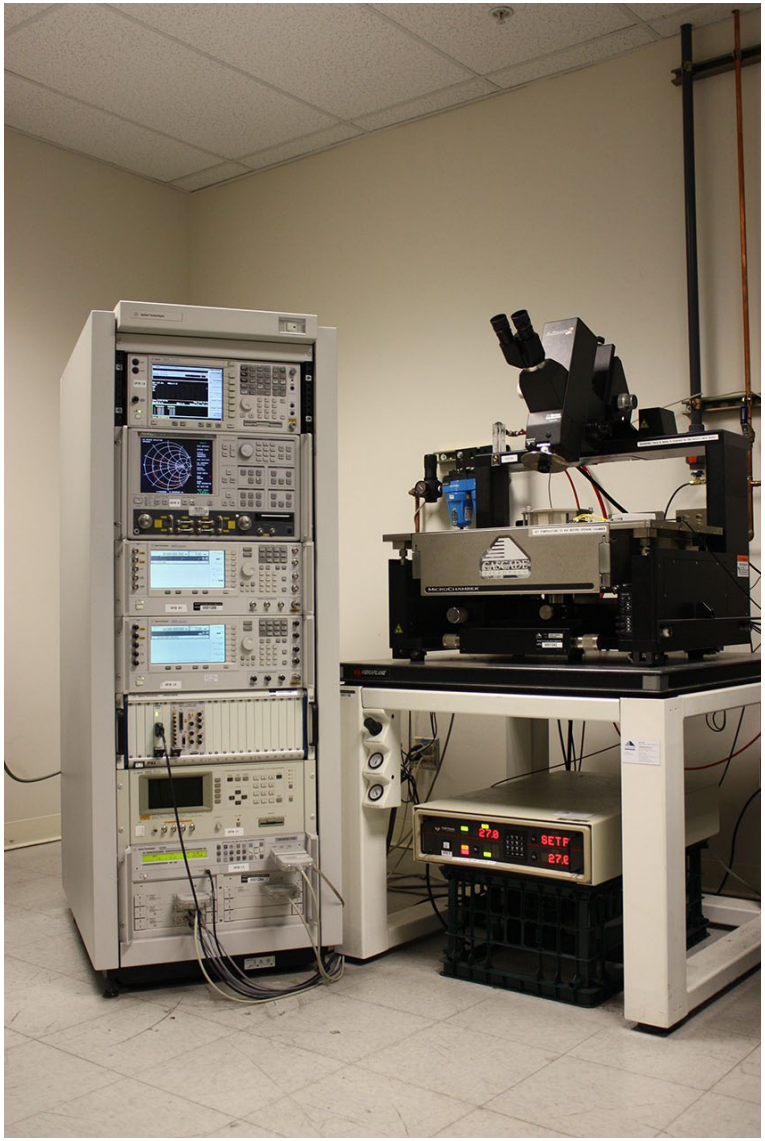
Bench testing used to qualify parts for production

Most integrated circuits are tested twice during production

- Wafer Probe Testing
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts
- Packaged Part Testing
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts

Bench Test Environment





Photos from www postings and Google image search

Bench Test Environment

Photo courtesy of Texas Instruments

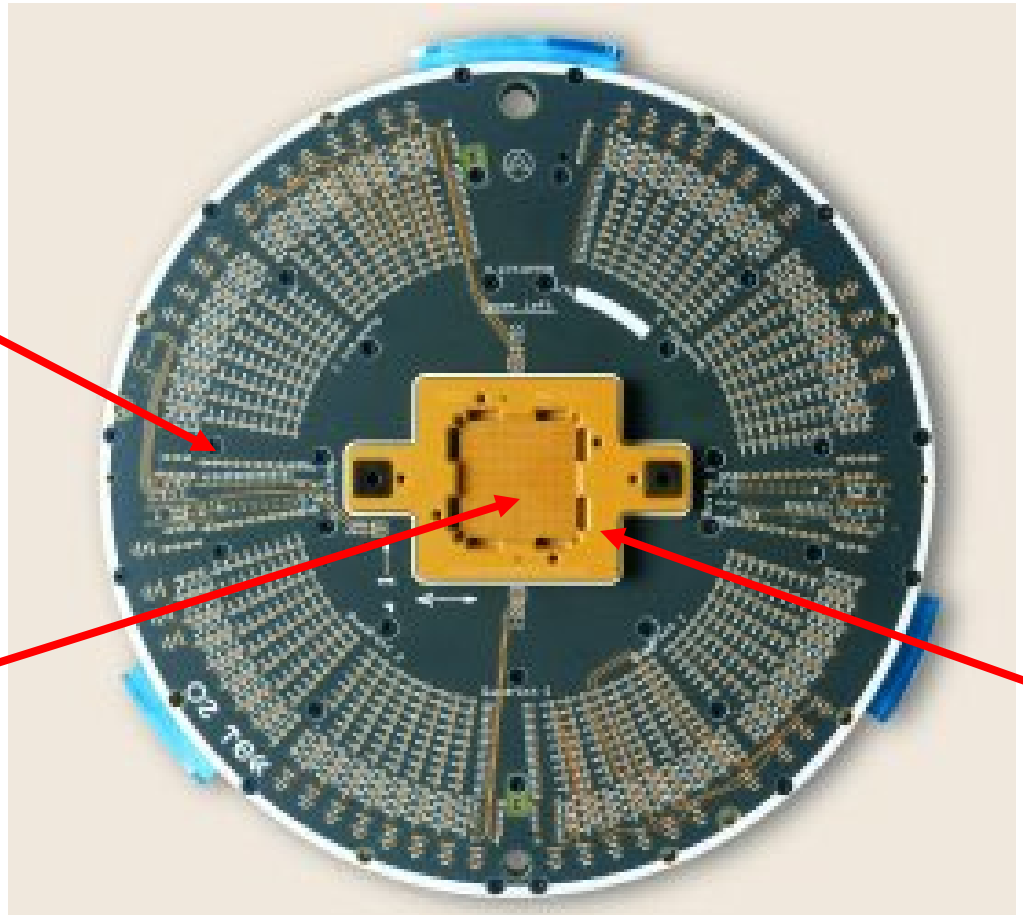
Final Test

Typical ATE System (less handler)

Automated Test Equipment (ATE)

Device Interface Board - DIB

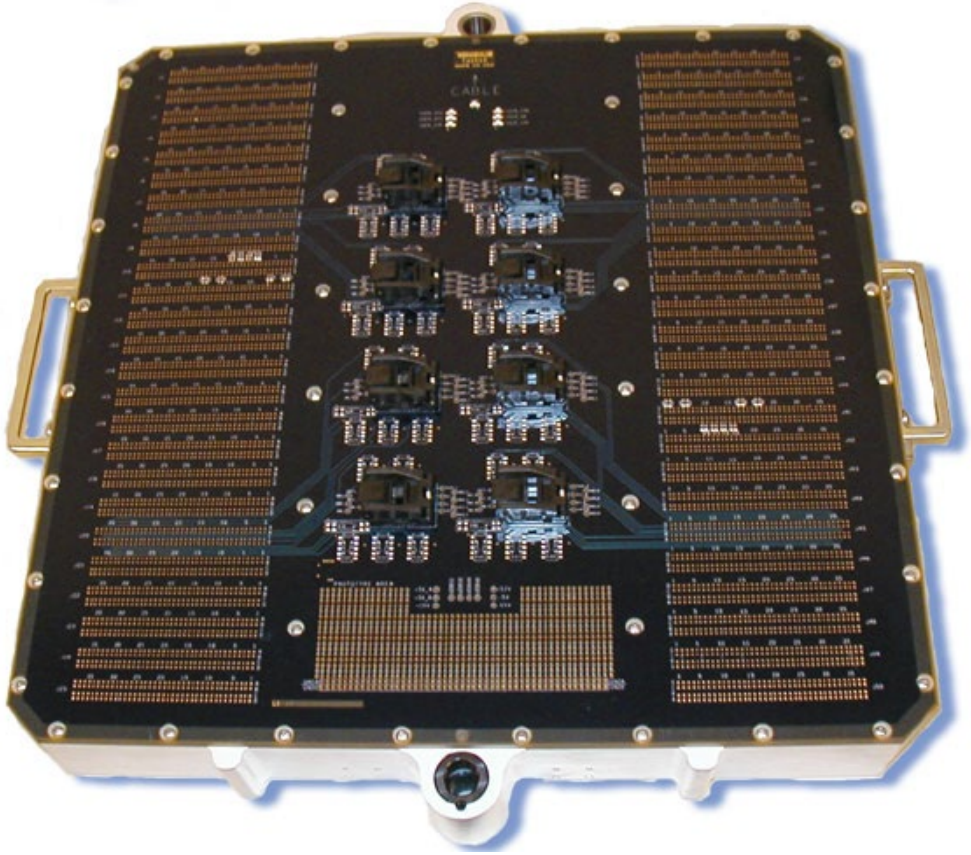
(Load Board)



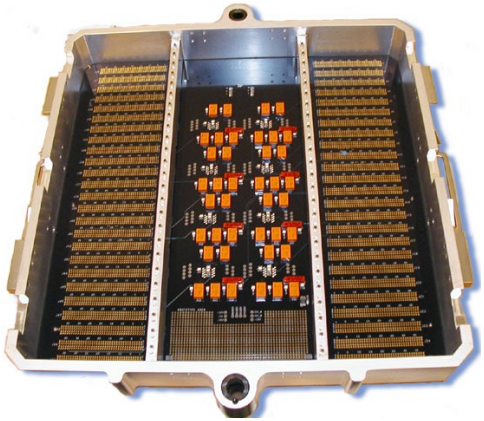
DIBs Vary Considerably from one ATE Platform to another and are often personalized for a particular DUT

Octal Site DIB

Flex Octal (Teradyne)



Top



Bottom

Final Test

Typical ATE Configuration

Handler

Tester

Test Head

Atlas (SSI Robotics)

Basic Semiconductor Processes

MOS (Metal Oxide Semiconductor)

1. NMOS n-ch
2. PMOS p-ch
3. CMOS n-ch & p-ch

- Basic Device: MOSFET
- Niche Device: MESFET
- Other Devices: Diode
  BJT (Bipolar Junction Transistor)
  JFET (Junction Field Effect Transistor)
  Resistors
  Capacitors
  Schottky Diode

Basic Semiconductor Processes

Bipolar

1. T^2L
2. ECL
3. I^2L
4. Linear Ics

- Basic Device: BJT (Bipolar Junction Transistor)
- Niche Devices: HBT (Heterojunction Bipolar Transistor)
- Other Devices: Diode
  Resistor
  Capacitor
  Schottky Diode
  JFET (Junction Field Effect Transistor)

Basic Semiconductor Processes

Other Processes

- Thin and Thick Film Processes
  - Basic Device: Resistor
- BiMOS or BiCMOS
  - Combines both MOS & Bipolar Processes
  - Basic Devices: MOSFET & BJT
- SiGe
  - BJT with HBT implementation
- SiGe / MOS
  - Combines HBT & MOSFET technology
- SOI / SOS (Silicon on Insulator / Silicon on Sapphire)
- Twin-Well & Twin Tub CMOS
  - Very similar to basic CMOS but more optimal transistor char.

Basic Devices

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (decent in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel

Primary Consideration in This Course

- Standard Bipolar Process
  - BJT
    - npn
    - pnp
  - JFET
    - n-channel
    - p-channel
  - Diodes
  - Resistors
  - Capacitors

Some Consideration in This Course

(devices are available in some CMOS processes)

- Niche Devices
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET
  - HBT
  - Schottky Diode (not Shockley)
  - MEM Devices
  - TRIAC/SCR
  - ….

Some Consideration in This Course

Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
- JFET
- MESFET

Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

Resistors were discussed when considering interconnects so will only be briefly reviewed here

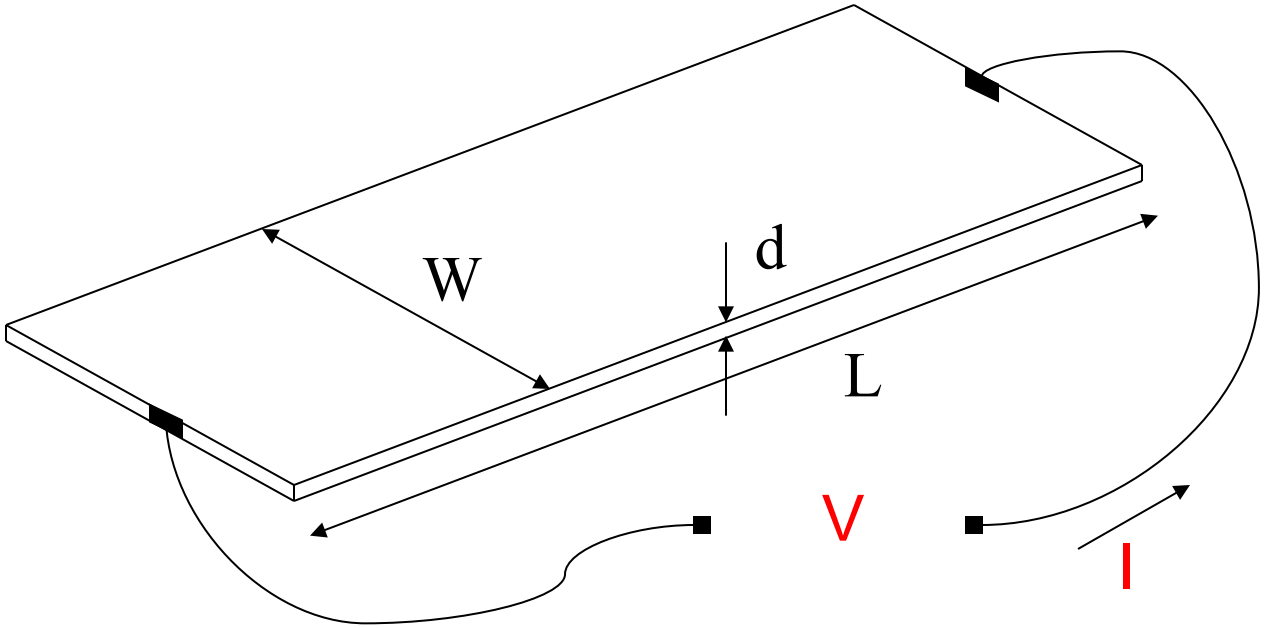
Resistors

- Generally thin-film devices
- Almost any thin-film layer can be used as a resistor
  - Diffused resistors
  - Poly Resistors
  - Metal Resistors
  - “Thin-film” adders (SiCr or NiCr)
- Subject to process variations, gradient effects and local random variations
- Often temperature and voltage dependent
  - Ambient temperature
  - Local Heating
- Nonlinearities often a cause of distortion when used in circuits
- Trimming resistors is possible
  - Laser, links, switches

Have already modeled resistance as an interconnect

Modeling is the same as for a resistor so will briefly review

Resistor Model

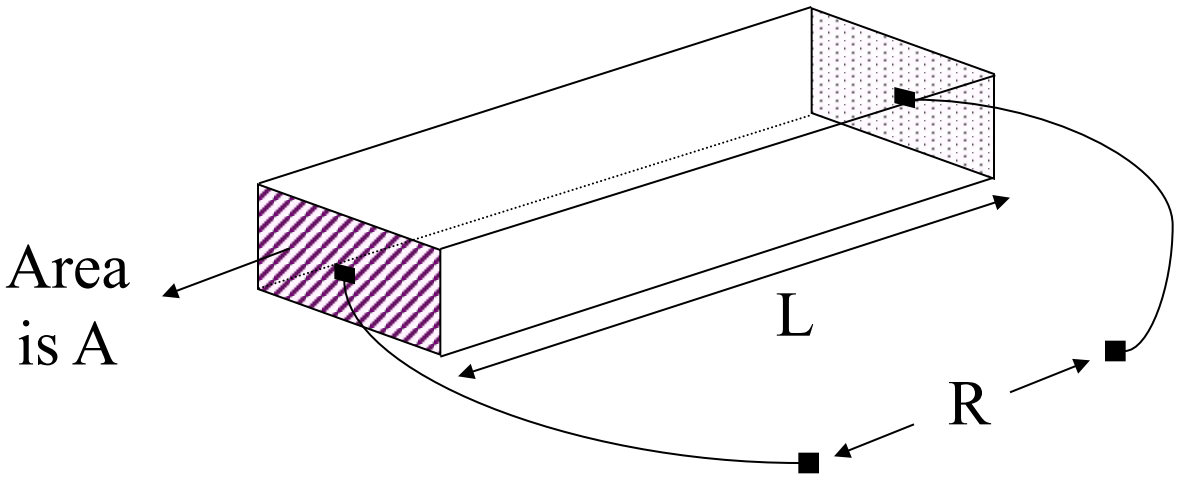


Model:

$$R = \frac{V}{I}$$

Resistivity

- Volumetric measure of conduction capability of a material

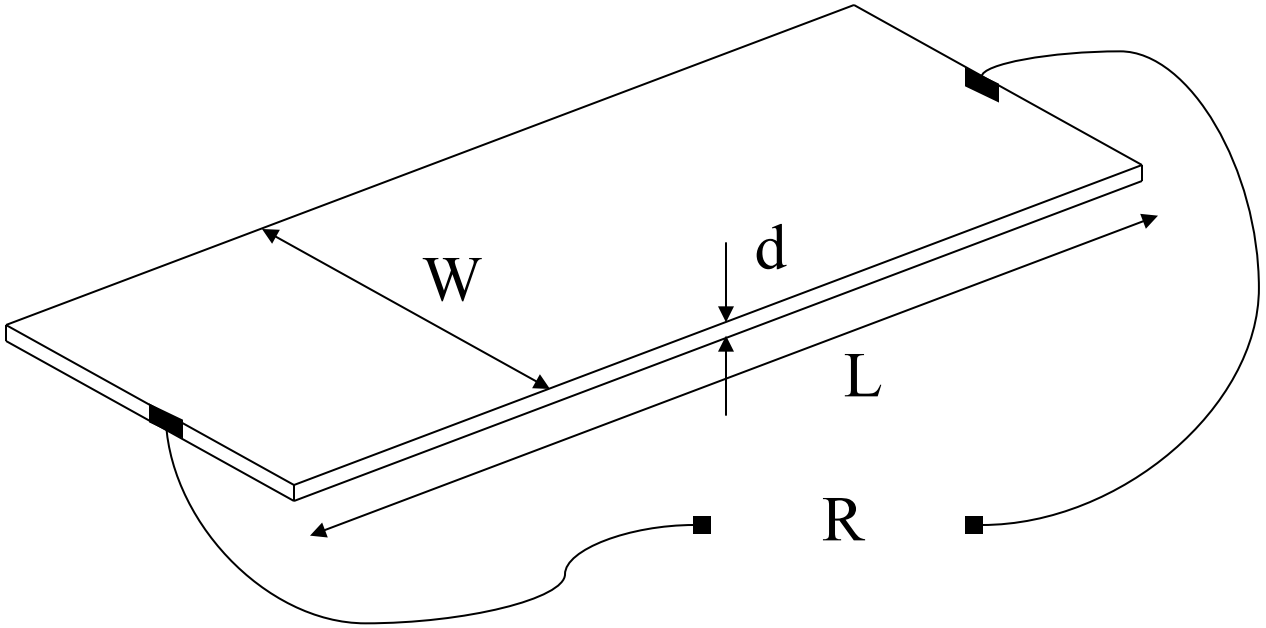


$$\rho = \frac{AR}{L}$$

units : ohm cm

for homogeneous material,
$\rho \perp A, R, L$

Sheet Resistance



$$R_{\square} = \frac{RW}{L} \quad (\text{ for } d << w,\ d << L\ ) \qquad \text{units : ohms / } \square$$

for homogeneous materials, $R_{\square}$ is independent of W, L, R

Relationship between ρ and $R_{□}$

$$R_{□} = \frac{RW}{L}$$

$$\rho = \frac{AR}{L}$$

$$\rho = \frac{A}{W} R_{□}$$

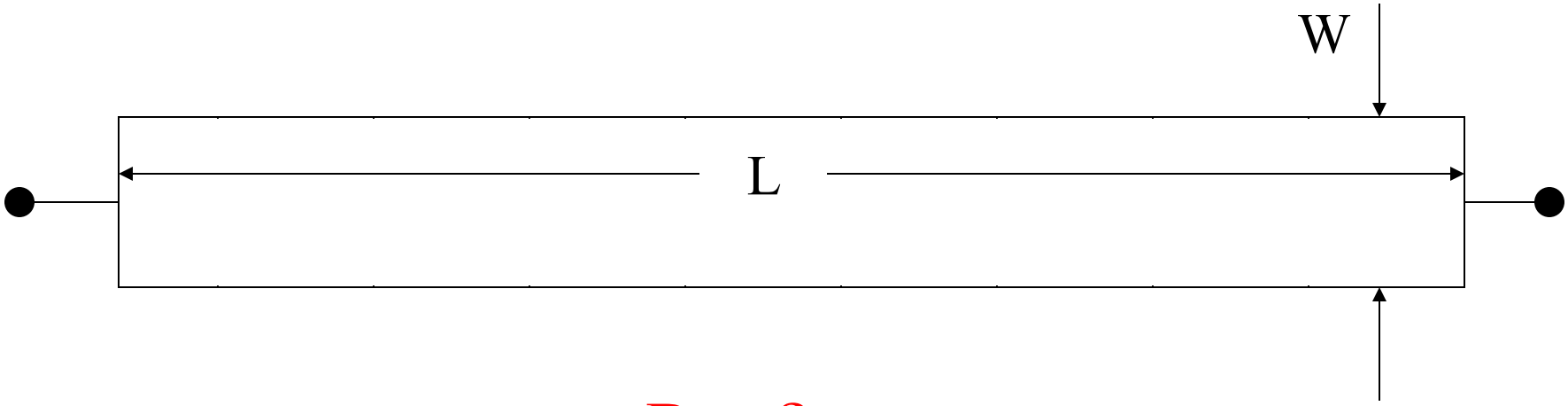
$$A = W \times d$$

$$\rho = \frac{A}{W} R_{□} = \frac{W\,d}{W} R_{□} = d \times R_{□}$$

Number of squares, N_S, often used instead of L / W in determining resistance of film resistors

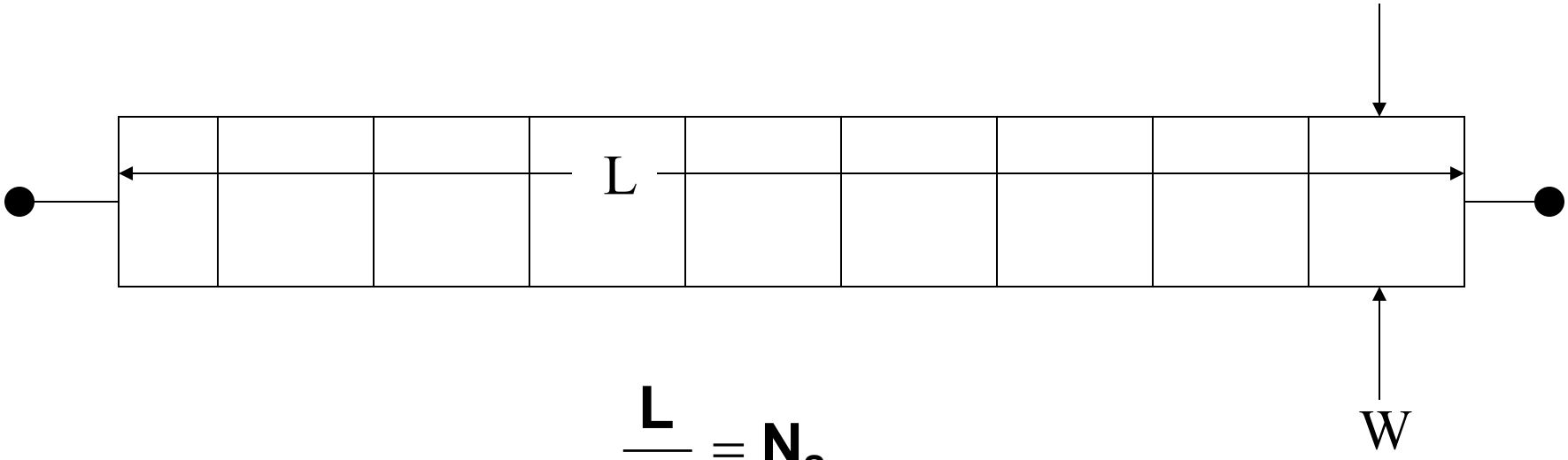
$$R = R_{□} N_S$$

Example 1



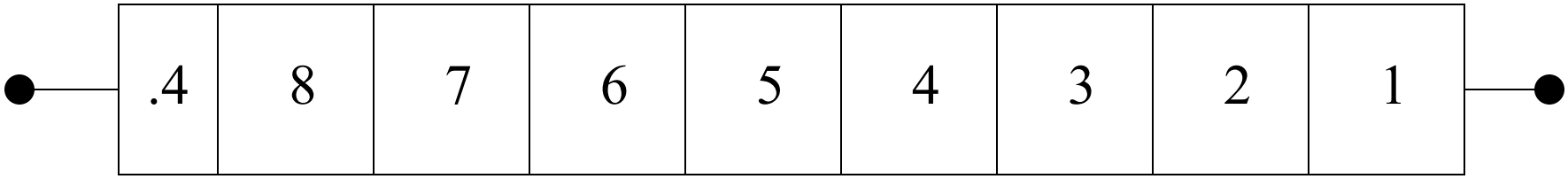
R = ?

Example 1



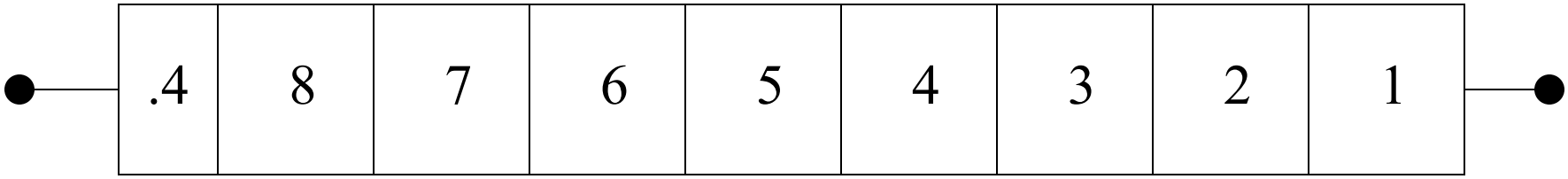
$$\frac{\mathbf{L}}{\mathbf{W}} = \mathbf{N_S}$$

Example 1



R = ?

Example 1

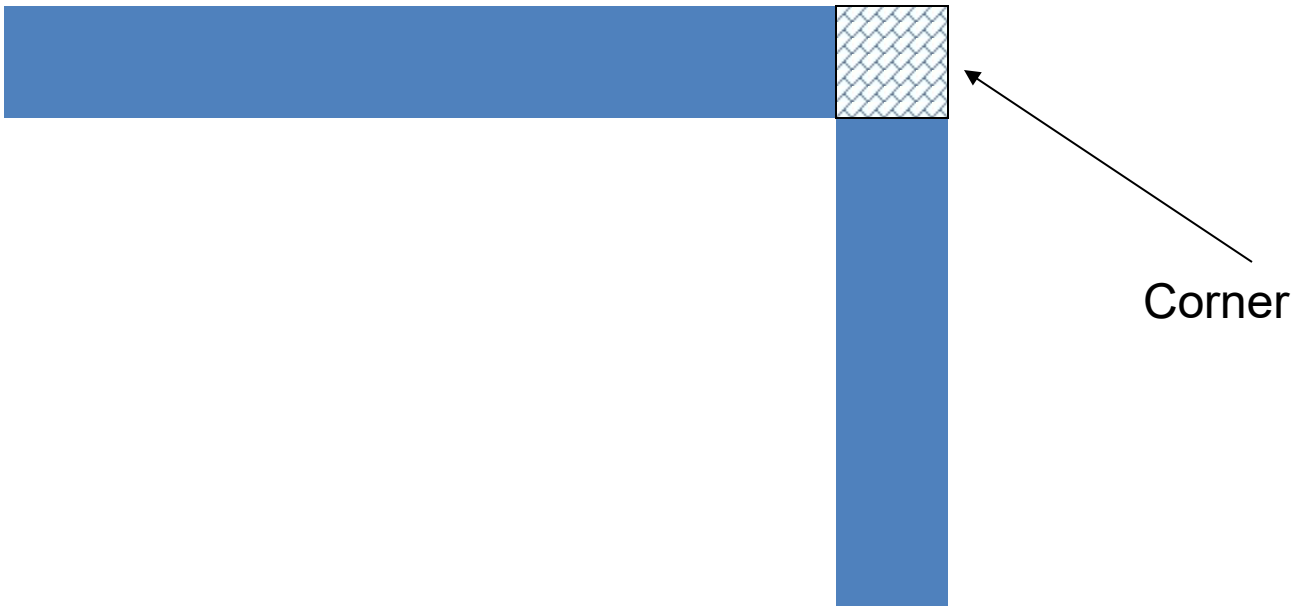


$R = ?$

$N_S = 8.4$

$R = R_{\square}(8.4)$

Corners in Film Resistors

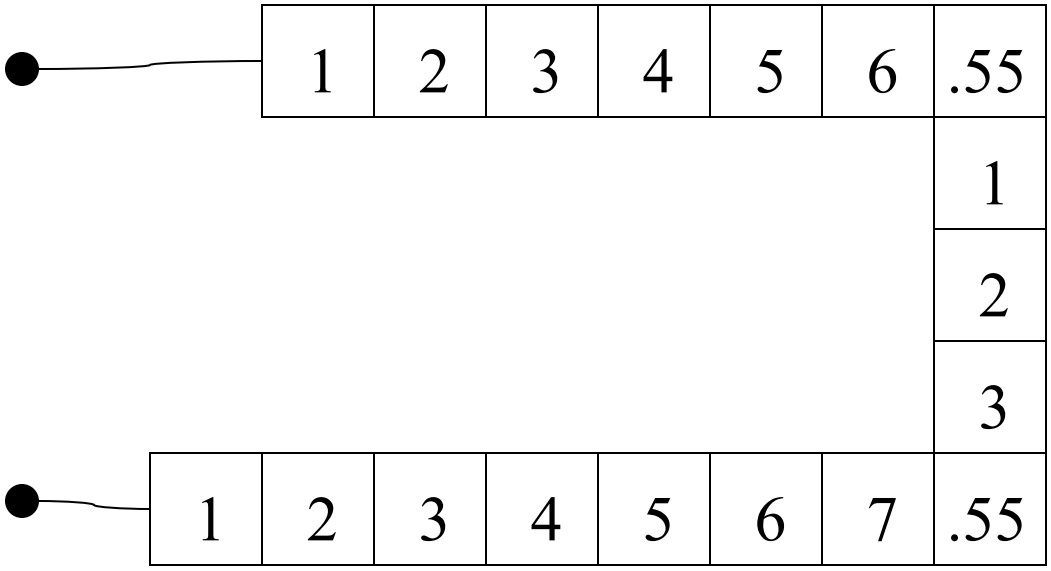


Rule of Thumb: .55 squares for each corner

Example 2

Determine R if $R_{\square} = 100\ \Omega / \square$

Example 2



$N_S = 17.1$

$R = (17.1)\ R_{\square}$

$R = 1710\ \Omega$

Resistivity of Materials used in Semiconductor Processing

- Cu: 1.7*E*-6 Ωcm
- Al: 2.7*E*-6 Ωcm
- Gold: 2.4*E*-6 Ωcm
- Platinum: 1.1*E*-5 Ωcm
- Polysilicon: 1E-2 to 1E4 Ωcm*
- n-Si: typically .25 to 5 Ωcm* (but larger range possible)
- intrinsic Si: 2.5*E5* Ωcm
- SiO_2: *E*14 Ωcm

* But fixed in a given process

http://www.cleanroom.byu.edu/ResistivityCal.phtml

Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant: (•) Arsenic ( ) Boron ( ) Phosphorus

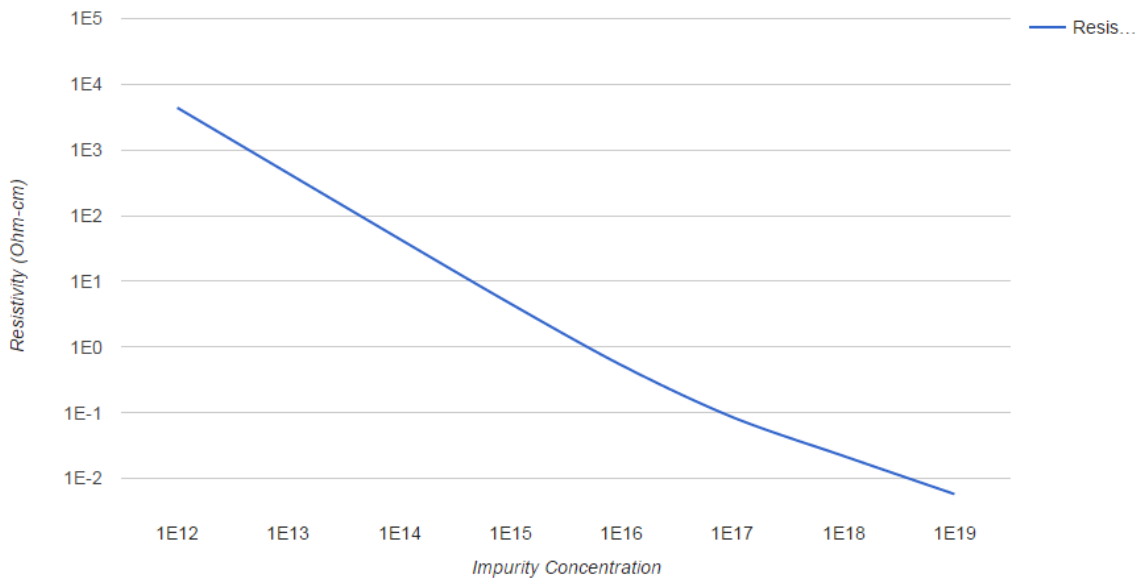
Impurity Concentration: 1e15 (cm^{-3})

Calculate | Export to CSV

Mobility: 1358.6941377290254 [$cm^2/V\text{-}s$]

Resistivity: 4.593746148183427 [$\Omega\text{-}cm$]

Calculations are for a silicon substrate.



http://www.cleanroom.byu.edu/ResistivityCal.phtml

Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- ○ Arsenic
- ◉ Boron
- ○ Phosphorus

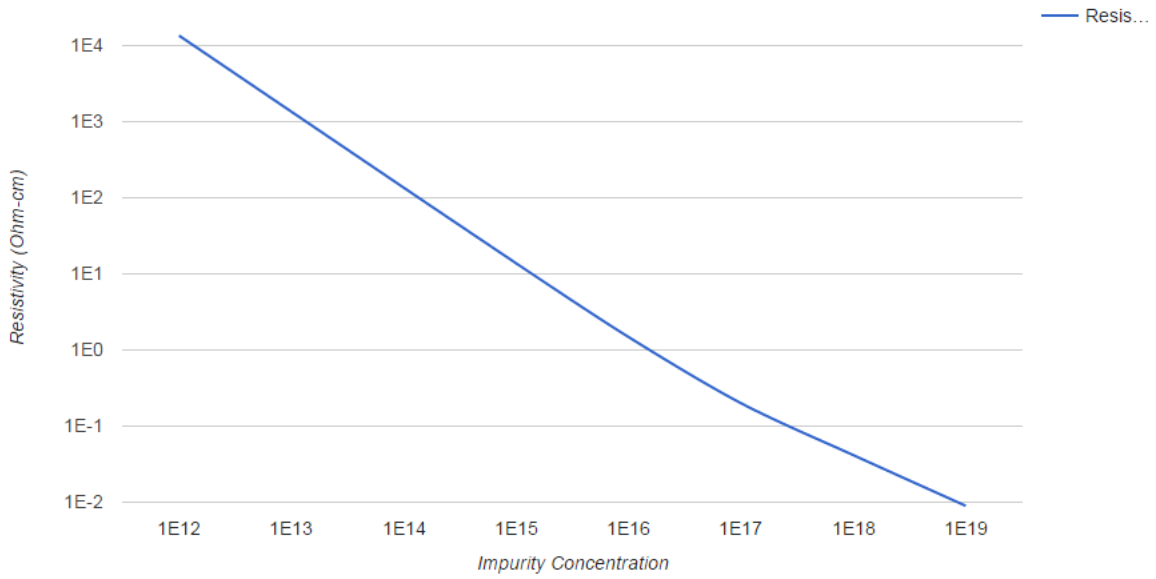
Impurity Concentration: 1e15 (cm^{-3})

Calculate | Export to CSV

Mobility: 461.9540345952693 [$cm^2/V\text{-}s$]

Resistivity: 13.511075765839905 [$\Omega\text{-}cm$]

Calculations are for a silicon substrate.



http://www.cleanroom.byu.edu/ResistivityCal.phtml

Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- ○ Arsenic
- ○ Boron
- ◉ Phosphorus

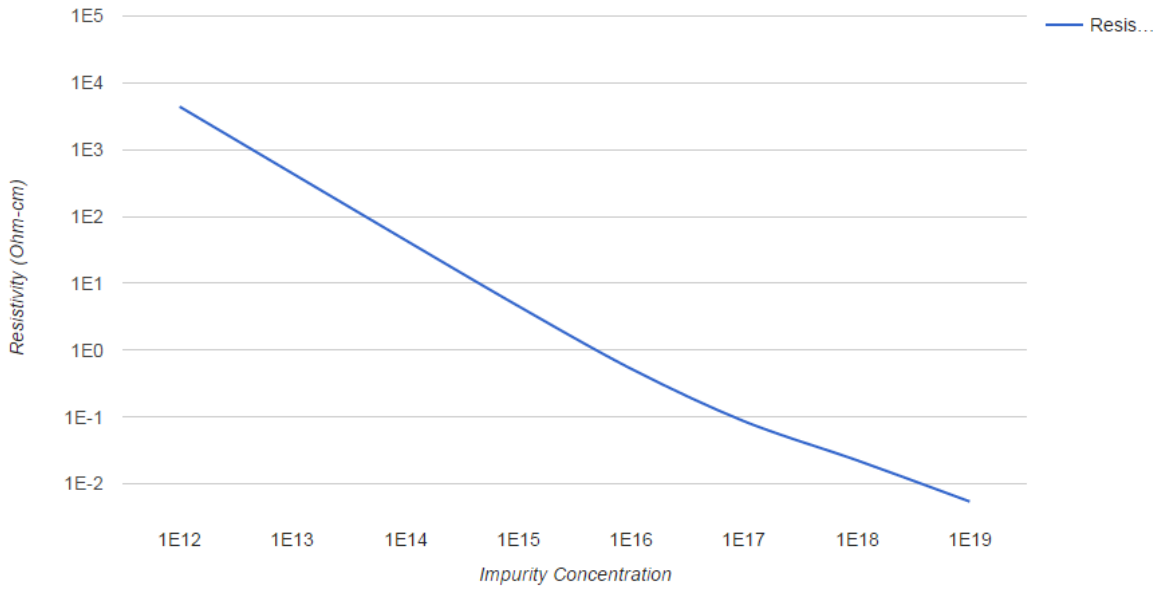
Impurity Concentration: 1e15 (cm^{-3})

Calculate | Export to CSV

Mobility: 1362.0563795030084 [$cm^2/V\text{-}s$]

Resistivity: 4.582406466925789 [Ω-cm]

Calculations are for a silicon substrate.



Temperature Coefficients

Used for indicating temperature sensitivity of resistors & capacitors

For a resistor:

$$\mathbf{TCR} = \left(\frac{\mathbf{1}}{\mathbf{R}} \frac{\mathbf{dR}}{\mathbf{dT}} \right)\Bigg|_{\mathbf{op.\ temp}} \bullet \mathbf{10^6\ ppm/^\circ C}$$

This differential eqn can easily be solved if TCR is a constant

$$R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6} TCR}$$

If x is small, $e^x \cong 1 + x$

It follows that If $TCR*(T_2-T_1)$ is small,

$$R(T_2) \approx R(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right]$$

Identical Expressions for Capacitors

Voltage Coefficients

Used for indicating voltage sensitivity of resistors & capacitors

For a resistor:

$$\mathbf{VCR} = \left(\frac{1}{R} \frac{dR}{dV} \right)\Bigg|_{\text{ref voltage}} \bullet 10^6 \text{ ppm/V}$$

This diff eqn can easily be solved if VCR is a constant

$$R(V_2) = R(V_1)\, e^{\frac{V_2 - V_1}{10^6} VCR}$$

It follows that If VCR*(V_2-V_1) is small,

$$R(V_2) \approx R(V_1)\left[1 + (V_2 - V_1)\frac{VCR}{10^6} \right]$$

Identical Expressions for Capacitors

Temperature and Voltage Coefficients

- Temperature and voltage coefficients often quite large for diffused resistors
- Temperature and voltage coefficients often quite small for poly and metal film (e.g. SiCr) resistors

Type of layer	Sheet Resistance Ω/□	Accuracy (absolute) %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

(relative accuracy much better and can be controlled by designer)

From:F. Maloberti : Design of CMOS Analog Integrated Circuits - “Resistors, Capacitors, Switches”

MOS Passive RC Component Typical Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOSFET gate Cap.	6-7 fF/μm^2	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm^2	20%	0.1%	25ppm/°C	±50ppm/V
Metal-Metal Capacitor	0.1-1fF/μm^2	10%	0.6%	-40ppm/°C	±1ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V
Top Metal Resistor	30 mΩ/sq.	15%	2%	4000ppm/°C	-
Lower Metal Resistor	70 mΩ/sq.	28%	3%	4000ppm/°C	-

Table 2.4-1 Approximate Performance Summary of Passive Components in a 0.18 μm CMOS Process

Component Type	Typical Value	Typical Matching Accuracy	Temperature Coefficient	Voltage Coefficient
MiM capacitor	1.0 fF/μm^2	0.03%	50 ppm/°C	50 ppm/V
MOM capacitor	0.17 fF/μm^2	1%	50 ppm/°C	50 ppm/V
P^+ Diffused resistor (nonsilicide)	80–150 Ω/□	0.4%	1500 ppm/°C	200 ppm/V
N^+ Diffused resistor (non-silicide)	50–80 Ω/□	0.4%	1500 ppm/°C	200 ppm/V
N^+ Poly resistor (non-silicide)	300 Ω/□	2%	−2000 ppm/°C	100 ppm/V
P^+ Poly resistor (non-silicide)	300 Ω/□	0.5%	−500 ppm/°C	100 ppm/V
P^- Poly resistor (non-silicide)	1000 Ω/□	0.5%	−1000 ppm/°C	100 ppm/V
n-well resistor	1–2 kΩ/□		8000 ppm/°C	10k ppm/V

From Allen Holberg Third Edition

MOS Passive RC Component Performance Summary

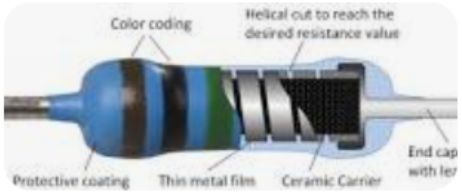
Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semi-conductor Capacitor	0.35-0.5 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

From ECE 6440 Lecture by P. Allen

Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

How does TCR of Integrated Resistors Compare with Low-Cost Discrete Resistors?

Metal film resistors are available with tolerances of 0.1, 0.25, 0.5, 1 and 2%. The temperature coefficient of resistance (TCR) is usually **between 50 and 100 ppm/°C**.



Integrated resistors typically have a much larger TCR but there are some special processes that provide resistors with excellent thermal stability ($$$)

Example: Determine the percent change in resistance of a 5K Polysilicon resistor as the temperature increases from 30°C to 60°C if the TCR is constant and equal to 1500 ppm/°C

$$R(T_2) \cong R(T_1)\left[1+(T_2-T_1)\frac{TCR}{10^6}\right]$$

$$R(T_2) \cong R(T_1)\left[1+(30^oC)\frac{1500}{10^6}\right]$$

$$R(T_2) \cong R(T_1)[1+.045]$$

$$R(T_2) \cong R(T_1)[1.045]$$

Thus the resistor increases by 4.5%

Did not need $R(T_1)$ to answer this question !

What is $R(T_1)$ as stated in this example ? 5K?

It is around 5K but if we want to be specific, would need to specify T

Stay Safe and Stay Healthy !

End of Lecture 12